Module 3: Small-Signal Analysis and Frequency Response of Amplifiers (Low Frequency)

Module 3 Overview: This module delves into the crucial technique of small-signal analysis, a fundamental tool for understanding and designing electronic amplifiers. We will explore how to analyze amplifier behavior for small AC signals, focusing specifically on low-frequency operation. The module will cover the development of AC equivalent circuits, introduce widely used small-signal models for Bipolar Junction Transistors (BJTs) and Field-Effect Transistors (FETs), and demonstrate how to calculate key amplifier parameters such as voltage gain, input resistance, and output resistance for various configurations. Finally, we will apply these concepts to multistage amplifiers and discuss practical design considerations.

3.1 AC Equivalent Circuits: Concept of Small-Signal Analysis

Introduction: Electronic amplifiers are designed to magnify small input signals. While DC biasing establishes the operating point (Q-point) of the transistor, it's the AC signal that carries the information we want to amplify. Small-signal analysis is a powerful technique that allows us to simplify the complex non-linear behavior of transistors into a linear model, valid for small variations around the DC operating point. This linearity is crucial because it allows us to use superposition and other linear circuit analysis techniques.

Concept of Small-Signal Analysis: The core idea behind small-signal analysis is linearization. A transistor, whether BJT or FET, is a non-linear device. Its output current is not directly proportional to its input voltage or current over a wide range. However, if the AC input signal is small enough, the transistor's operating point effectively "moves" within a very small, approximately linear region of its characteristic curves. Within this small region, the transistor can be modeled as a linear circuit element.

Steps for Small-Signal Analysis:

1. **Determine the DC Operating Point (Q-point):** First, the DC bias voltages and currents for the transistor must be found. This defines the quiescent state around which the AC signals will vary. This step involves setting all AC sources to zero (shorting AC voltage sources and opening AC current sources) and analyzing the DC equivalent circuit.
2. **Replace DC Voltage Sources with Shorts and DC Current Sources with Opens:** For AC analysis, all DC voltage sources are considered ideal shorts because they present zero impedance to AC signals. Similarly, ideal DC current sources are considered open circuits. This is a critical simplification for creating the AC equivalent circuit.
3. **Replace Capacitors with Shorts:** At the low frequencies we are considering in this module, coupling and bypass capacitors are assumed to have negligible impedance.

Therefore, they are treated as short circuits for AC signals. This allows AC signals to pass through while blocking DC.

4. **Replace Transistors with Their Small-Signal Models:** This is the most crucial step. The non-linear transistor is replaced by a linear equivalent circuit model (e.g., π-model or T-model for BJTs, or small-signal models for FETs). These models consist of resistors, dependent sources, and sometimes capacitors (though capacitors are often neglected for low-frequency analysis, as we are doing here). The parameters of these models are determined by the DC operating point.
5. **Analyze the Resulting AC Equivalent Circuit:** Once the circuit is transformed into its AC equivalent, standard linear circuit analysis techniques (Kirchhoff's laws, voltage dividers, current dividers, Thevenin/Norton equivalents, etc.) can be applied to determine AC voltage gain, current gain, input resistance, and output resistance.

Why "Small" Signal? The term "small" refers to the amplitude of the AC signal. If the AC signal is too large, the transistor's operation will swing beyond the linear region, and the small-signal model will no longer accurately represent its behavior, leading to distortion. Generally, an AC voltage is considered "small" if it causes variations in terminal voltages and currents that are significantly less than the DC bias values, ensuring the linear approximation holds. For example, for a BJT, the AC base-emitter voltage v_be should be much less than the thermal voltage V_T (approximately 25 mV at room temperature).

3.2 Low-Frequency BJT Models: π-Model and T-Model

Introduction: To perform small-signal analysis on BJT circuits, we need a linear equivalent circuit that represents the transistor's behavior for small AC signals. The two most commonly used low-frequency small-signal models for BJTs are the hybrid-π (π-model) and the T-model. Both models accurately represent the BJT's AC characteristics, but one might be more convenient depending on the specific circuit configuration.

Key Parameters for BJT Small-Signal Models: These parameters are crucial for defining the components within the small-signal models and are dependent on the DC operating point.

- **Transconductance (g_m):** This parameter relates the change in collector current (i_c) to a change in base-emitter voltage (v_be). It signifies how effectively the input voltage controls the output current.
  $g_m = \frac{I_C}{V_T}$
  Where:
  - I_C is the DC collector current at the Q-point.
  - V_T is the thermal voltage, approximately 25 mV at room temperature.
- **Input Resistance at the Base (r_pi):** This resistance represents the dynamic resistance seen looking into the base-emitter junction.
  $r_\pi = \frac{\beta}{g_m} = \frac{\beta V_T}{I_C}$
  Where:
  - beta (beta) is the common-emitter current gain, obtained from the transistor's datasheet or DC analysis. It is often denoted as h_fe.

- **Output Resistance (r_o):** This resistance accounts for the Early effect, which describes the slight increase in collector current with increasing collector-emitter voltage even when the base-emitter voltage is constant. It represents the resistance seen looking into the collector, parallel to the current source.
  $r_o = \left| \frac{V_A}{I_C} \right| = \frac{V_A + V_{CEQ}}{I_C} \approx \frac{V_A}{I_C}$
  Where:
  - V_A is the Early voltage, a transistor parameter (typically 50-100 V).
  - V_{CEQ} is the DC collector-emitter voltage at the Q-point. In many practical cases, if $V_A \gg V_{CEQ}$, r_o can be approximated as V_A/I_C. If not specified, r_o is often assumed to be infinite (open circuit) for simpler analysis, especially in introductory contexts.

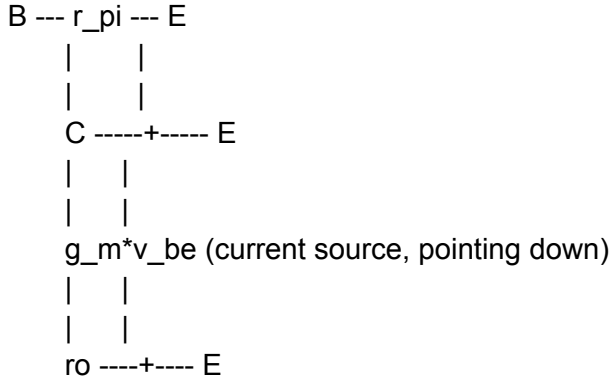
3.2.1 The π-Model (Hybrid-π Model)

The π-model is widely used and provides a good representation of the BJT's AC behavior.

Components of the π-Model:

- **r_pi:** Resistor between the base and emitter, representing the dynamic input resistance.
- **g_mv_be:** Dependent current source from collector to emitter, representing the transconductance effect, where v_be is the AC voltage across r_pi.
- **r_o:** Resistor between collector and emitter, representing the output resistance due to the Early effect.

Diagram of the π-Model:



(Self-Correction: The above is a textual representation. In a real course, a clear circuit diagram would be essential here.)

Explanation of Components:

- The input side of the model consists of r_pi between base and emitter. Any AC voltage applied between base and emitter (v_be) will cause a current to flow through r_pi.

- This v_be controls the dependent current source g_mv_be that flows from the collector to the emitter. This is the amplifier's fundamental action: a small input voltage causes a significant output current.
- The output resistance r_o is connected in parallel with the current source between collector and emitter.

Advantages of the π-Model:

- Intuitive representation of the input resistance (r_pi) and transconductance (g_m).
- Widely used in higher-frequency analysis (though not covered in this low-frequency module).

3.2.2 The T-Model

The T-model is an alternative to the π-model, often simpler for analyzing circuits with an emitter resistor.

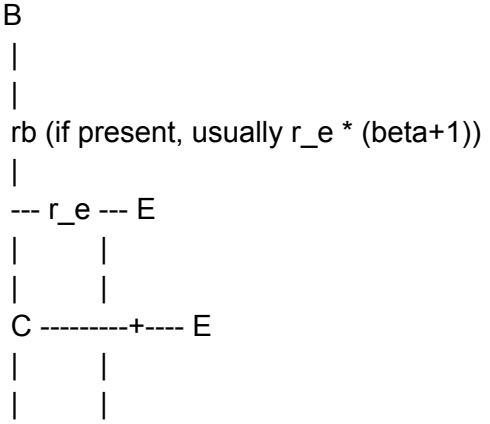
Key Parameter for T-Model:

- **Emitter Resistance (r_e):** This resistance represents the dynamic resistance seen looking into the emitter.
  re=IEVT=gmα
  Where:
  - I_E is the DC emitter current at the Q-point.
  - alpha (alpha) is the common-base current gain, where alpha=fracbetabeta+1. Since I_EapproxI_C, r_eapproxfracV_TI_C=frac1g_m.

Components of the T-Model:

- **r_e:** Resistor in series with the emitter, representing the dynamic resistance seen looking into the emitter.
- **alphai_e:** Dependent current source from collector to emitter, controlled by the AC emitter current i_e. (Alternatively, g_mv_be can still be used, with v_be=i_er_e).
- **r_o:** Resistor between collector and emitter, representing the output resistance.

Diagram of the T-Model:



alpha*i_e (current source, pointing down)
| |
| |
ro --------+---- E

(Self-Correction: Again, a proper circuit diagram is needed in the actual course material.)

Explanation of Components:

- The emitter resistance r_e is placed directly in the emitter path.
- The dependent current source is either alphai_e (proportional to emitter current) or g_mv_be (proportional to base-emitter voltage, where v_be is the voltage across r_e and any other series resistance from base to emitter).
- r_o remains connected between collector and emitter.

Advantages of the T-Model:

- Often simplifies analysis of circuits with emitter resistors, such as common-collector configurations.
- The resistance seen looking into the emitter is directly r_e.

Numerical Example for BJT Models: Consider a BJT operating at a DC collector current I_C=1mA with beta=100 and V_A=75V. Assume V_T=25mV.

Calculate Small-Signal Parameters:

1. **Transconductance (g_m):**
   g_m=fracI_CV_T=frac1textmA25textmV=frac1times10−3textA25times10−3textV=0.04textA/V=40textmS
2. **Input Resistance at the Base (r_pi):**
   r_pi=fracbetag_m=frac1000.04textA/V=2500textOmega=2.5textkOmega
3. **Emitter Resistance (r_e):**
   r_e=fracV_TI_EapproxfracV_TI_C=frac25textmV1textmA=25textOmega
   Alternatively,
   r_e=fracalphag_m=fracbeta/(beta+1)g_m=frac100/10140textmSapprox0.99times25textOmegaapprox24.75textOmega. The approximation r_eapproxV_T/I_C is often sufficient.
4. **Output Resistance (r_o):**
   r_o=fracV_AI_C=frac75textV1textmA=frac751times10−3textOmega=75000textOmega=75textkOmega

These calculated values would then be used in the respective π-model or T-model for AC analysis.

3.3 Low-Frequency FET Models: Small-Signal Models for JFETs and MOSFETs

Introduction: Similar to BJTs, Field-Effect Transistors (FETs) also require small-signal models for AC analysis. FETs, including Junction FETs (JFETs) and Metal-Oxide-Semiconductor FETs (MOSFETs), are voltage-controlled devices, meaning their output current is controlled by an input voltage. Their small-signal models reflect this characteristic. A key difference from BJTs is that FETs have very high input impedance (ideally infinite) because their gate is isolated from the channel.

Key Parameters for FET Small-Signal Models: These parameters are derived from the DC operating point and are crucial for defining the components within the models.

- **Transconductance (g_m):** This parameter relates the change in drain current (i_d) to a change in gate-source voltage (v_gs). It indicates how effectively the input voltage controls the output current.
    - **For JFETs (in saturation):**

      $gm=\left|VP\right|22IDSS\left|VGSQ-VP\right|=VP2IDSSID$ 
      Where:
        - I_DSS is the drain current with gate shorted to source and V_DSge$\left|V_P\right|$.
        - V_P (or V_GS(off)) is the pinch-off voltage.
        - V_GSQ is the DC gate-source voltage at the Q-point.
        - I_D is the DC drain current at the Q-point.
    - **For n-MOSFETs (in saturation):**

      $gm=kn'LW(VGSQ-Vth)=2kn'LWID$ 
      Where:
        - k_n′ is the transconductance parameter for the n-channel device (device constant).
        - W/L is the width-to-length ratio of the MOSFET channel.
        - V_th is the threshold voltage.
        - V_GSQ is the DC gate-source voltage at the Q-point.
        - I_D is the DC drain current at the Q-point.
    - **For p-MOSFETs (in saturation):**

      $gm=kp'LW\left|VGSQ-Vth\right|=2kp'LWID$ 
      (Similar formula to n-MOSFET, with appropriate signs for V_GSQ and V_th).
- **Output Resistance (r_o):** This resistance accounts for channel-length modulation, which describes the slight increase in drain current with increasing drain-source voltage, even when V_GS is constant.
  $ro=\lambda ID1=ID\left|VA\right|$
  Where:

    - lambda (lambda) is the channel-length modulation parameter (typically 0.01textV−1 to 0.1textV−1).
    - V_A=1/lambda is the Early voltage for FETs (not the same as BJT Early voltage, but conceptually similar).
    - I_D is the DC drain current at the Q-point. If not specified, r_o is often assumed to be infinite (open circuit) for simpler analysis.

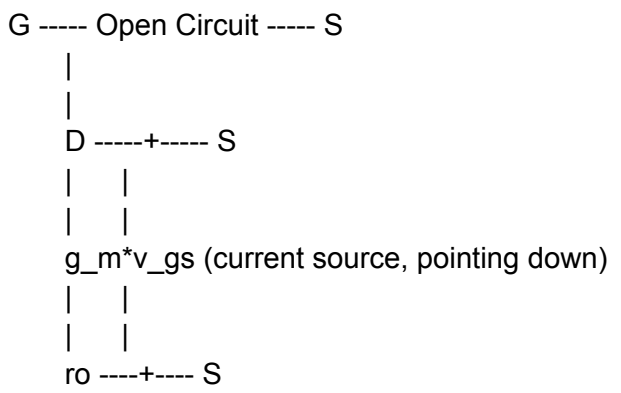
3.3.1 General Small-Signal FET Model

The small-signal model for JFETs and MOSFETs is essentially the same at low frequencies, only differing in how g_m and r_o are calculated.

Components of the Small-Signal FET Model:

- **Open Circuit at Gate-Source:** Ideally, the input resistance at the gate is infinite (open circuit), meaning no AC current flows into the gate.
- **g_mv_gs:** Dependent current source from drain to source, representing the transconductance effect, where v_gs is the AC voltage between the gate and source.
- **r_o:** Resistor between drain and source, representing the output resistance due to channel-length modulation.

Diagram of the Small-Signal FET Model:



(Self-Correction: A proper circuit diagram is required for the course.)

Explanation of Components:

- The gate (G) is effectively an open circuit for AC signals relative to the source (S), reflecting the very high input impedance of FETs. Therefore, any AC voltage applied between gate and source (v_gs) does not draw current from the input.
- This v_gs controls the dependent current source g_mv_gs that flows from the drain (D) to the source (S). This is the fundamental amplifying action of the FET.
- The output resistance r_o is connected in parallel with the current source between drain and source.

Advantages of the FET Small-Signal Model:

- Simplicity due to the ideal infinite input impedance.
- Directly shows the voltage-controlled current source behavior.

Numerical Example for FET Models: Consider an n-MOSFET operating at a DC drain current I_D=2mA with k_n′(W/L)=4mA/V2 and V_th=1V. Assume lambda=0.02textV−1.

Calculate DC V_GSQ first (if not given): In saturation, I_D=frac12k_n′fracWL(V_GSQ−V_th)2. 2textmA=frac12(4textmA/V2)(V_GSQ−1textV)2 1=(V_GSQ−1)2 V_GSQ−1=pm1textV Since V_GSQV_th for saturation, V_GSQ−1=1, so V_GSQ=2textV.

Calculate Small-Signal Parameters:

1. **Transconductance (g_m):** g_m=k_n′fracWL(V_GSQ−V_th)=4textmA/V2(2textV−1textV)=4textmA/V=4textmS Alternatively, using the second formula: g_m=2sqrtk_n′fracWLI_D=2sqrt(4textmA/V2)(2textmA)=2sqrt8text(mA)2/textV2=2times2.828textmA/Vapprox5.66textmS. (The slight difference arises from using rounded values for k_n′(W/L) and I_D directly from the problem statement rather than deriving I_D precisely from a primary V_GSQ). We'll stick with the first calculation as it directly uses the derived V_GSQ.
2. **Output Resistance (r_o):** r_o=frac1lambdaI_D=frac1(0.02textV−1)(2textmA)=frac10.04textmS=frac10.04times10−3textA/V=25000textOmega=25textkOmega

These calculated values are used in the FET small-signal model for AC analysis.

3.4 Voltage Gain, Input Resistance, and Output Resistance Estimation

Introduction: Once the AC equivalent circuit is established by replacing DC sources, capacitors, and transistors with their small-signal models, we can analyze the amplifier's performance for AC signals. The key parameters of interest are voltage gain (A_v), input resistance (R_in), and output resistance (R_out). These parameters characterize how the amplifier modifies the input signal and how it interacts with preceding and succeeding stages.

General Definitions:

- **Voltage Gain (A_v):** The ratio of the AC output voltage to the AC input voltage. Av=vinvout
- **Input Resistance (R_in):** The equivalent resistance seen by the input signal source looking into the amplifier's input terminals. It determines how much current the input source has to supply. Rin=iinvin
- **Output Resistance (R_out):** The equivalent resistance seen by the load looking back into the amplifier's output terminals when the input signal is set to zero. It determines how much the output voltage will drop when a load is connected.

Rout=itestvtest(with vin=0)
To find R_out, we typically short-circuit independent voltage sources and open-circuit independent current sources at the input, then apply a test voltage (v_test) or current (i_test) at the output and calculate the resulting current or voltage.

Let's analyze these parameters for common amplifier configurations.

3.4.1 Common Emitter (CE) BJT Amplifier

Configuration Characteristics:

- **Input:** Applied to the base.
- **Output:** Taken from the collector.
- **Emitter:** AC grounded (either directly or via a large bypass capacitor).
- **Inverting:** The output voltage is typically 180 degrees out of phase with the input voltage.
- **High Voltage Gain:** Can provide significant voltage amplification.
- **Moderate Input Resistance:** Generally in the range of kOhms.
- **Moderate Output Resistance:** Generally in the range of kOhms.

AC Equivalent Circuit (Simplified, assuming r_o is infinite and no R_E or bypassed):
Input side: v_in connected to base, R_B (parallel combination of bias resistors) connected to base, r_pi between base and emitter (ground). Output side: Collector connected to R_C (load resistor) and g_mv_be current source. Emitter is AC ground.

Derivations (using π-model, assuming bypassed R_E if present, and r_o typically much larger than R_C):

1. **Voltage Gain (A_v):**
    - The AC voltage at the base is v_in. So, v_be=v_in.
    - The current flowing through the dependent source is g_mv_be=g_mv_in.
    - This current flows through R_C (and r_o in parallel, but r_oR_C often allows us to ignore r_o for gain calculation) to ground. The output voltage is across R_C.
    - v_out=−(g_mv_in)R_C (Negative sign indicates 180-degree phase shift).
    - Av=vinvout=−gmRC
      If r_o is considered, R_C is effectively in parallel with r_o. So, $R_L' = R_C || r_o$.
      $A_v = -g_m(R_C || r_o)$
2. **Input Resistance (R_in):**
    - Looking into the base, the input resistance is r_pi in parallel with any bias resistors connected to the base (e.g., R_1∣∣R_2).
    - $R_{in} = R_B || r_\pi$
    - Where R_B is the Thevenin equivalent resistance of the biasing network seen from the base (e.g., R_1∣∣R_2 for voltage divider bias).
3. **Output Resistance (R_out):**

    - Looking back into the collector, with the input set to zero (v_in=0impliesv_be=0impliesg_mv_be=0), the dependent current source becomes an open circuit.
    - The output resistance is then R_C in parallel with r_o.
    - Rout=RC||ro

Numerical Example for CE Amplifier: Consider a CE amplifier with R_C=4.7textkOmega, R_1||R_2=50textkOmega. Transistor parameters from previous example: g_m=40textmS, r_pi=2.5textkOmega, r_o=75textkOmega.

1. **Voltage Gain (A_v):** A_v=−g_m(R_C||r_o)=−40textmS(4.7textkOmega||75textkOmega) R_C||r_o=frac4.7times754.7+75textkOmega=frac352.579.7textkOmegaapprox4.42textkOmega A_v=−40times10−3textA/Vtimes4.42times103textOmega=−176.8
2. **Input Resistance (R_in):** R_in=(R_1||R_2)||r_pi=50textkOmega||2.5textkOmega R_in=frac50times2.550+2.5textkOmega=frac12552.5textkOmegaapprox2.38textkOmega
3. **Output Resistance (R_out):** R_out=R_C||r_o=4.7textkOmega||75textkOmegaapprox4.42textkOmega

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3.4.2 Common Source (CS) FET Amplifier

Configuration Characteristics:

- **Input:** Applied to the gate.
- **Output:** Taken from the drain.
- **Source:** AC grounded (either directly or via a large bypass capacitor).
- **Inverting:** Output typically 180 degrees out of phase with input.
- **High Voltage Gain:** Can provide significant voltage amplification.
- **Very High Input Resistance:** Ideally infinite due to isolated gate.
- **Moderate Output Resistance:** Generally in the range of kOhms.

AC Equivalent Circuit (Simplified, assuming r_o is infinite and no R_S or bypassed): Input side: v_in connected to gate, R_G (bias resistor) connected to gate. Gate is open circuit for current. Output side: Drain connected to R_D (load resistor) and g_mv_gs current source. Source is AC ground.

Derivations (using FET small-signal model, assuming bypassed R_S if present):

1. **Voltage Gain (A_v):**
    - The AC voltage at the gate is v_in. So, v_gs=v_in.
    - The current flowing through the dependent source is g_mv_gs=g_mv_in.
    - This current flows through R_D (and r_o in parallel, but r_oR_D often allows us to ignore r_o for gain calculation) to ground. The output voltage is across R_D.
    - v_out=−(g_mv_in)R_D (Negative sign indicates 180-degree phase shift).

    - $A_v = \frac{v_{in}}{v_{out}} = -g_m R_D$
      If r_o is considered, R_D is effectively in parallel with r_o. So, $R_L' = R_D || r_o$.
      $A_v = -g_m (R_D || r_o)$
2. **Input Resistance (R_{in}):**
    - Looking into the gate, the resistance is ideally infinite. However, practically, it is the gate bias resistor(s) to ground.
    - $R_{in} = R_G$
    - Where R_G is the bias resistor (or parallel combination of bias resistors, e.g., $R_1 || R_2$ for voltage divider bias).
3. **Output Resistance (R_{out}):**
    - Looking back into the drain, with the input set to zero ($v_{in} = 0 \implies v_{gs} = 0 \implies g_m v_{gs} = 0$), the dependent current source becomes an open circuit.
    - The output resistance is then R_D in parallel with r_o.
    - $R_{out} = R_D || r_o$

Numerical Example for CS Amplifier: Consider a CS amplifier with $R_D = 5\text{ k}\Omega$, $R_G = 1\text{ M}\Omega$. Transistor parameters from previous example: $g_m = 4\text{ mS}$, $r_o = 25\text{ k}\Omega$.

1. **Voltage Gain (A_v):**
   $A_v = -g_m (R_D || r_o) = -4\text{ mS} (5\text{ k}\Omega || 25\text{ k}\Omega)$
   $R_D || r_o = \frac{5 \times 25}{5 + 25}\text{ k}\Omega = \frac{125}{30}\text{ k}\Omega \approx 4.17\text{ k}\Omega$
   $A_v = -4 \times 10^{-3}\text{ A/V} \times 4.17 \times 10^3\ \Omega = -16.68$
2. **Input Resistance (R_{in}):** $R_{in} = R_G = 1\text{ M}\Omega$
3. **Output Resistance (R_{out}):**
   $R_{out} = R_D || r_o = 5\text{ k}\Omega || 25\text{ k}\Omega \approx 4.17\text{ k}\Omega$

3.4.3 Common Collector (CC) BJT Amplifier (Emitter Follower)

Configuration Characteristics:

- **Input:** Applied to the base.
- **Output:** Taken from the emitter.
- **Collector:** AC grounded (connected directly to VCC, which is AC ground).
- **Non-Inverting:** Output voltage is in phase with the input voltage.
- **Voltage Gain close to unity (but less than 1):** Provides current gain and impedance transformation, not voltage amplification.
- **High Input Resistance:** Useful for buffering high impedance sources.
- **Low Output Resistance:** Useful for driving low impedance loads.

AC Equivalent Circuit (using T-model often simplifies analysis for CC): Input side: v_{in} connected to base, R_B to base. Base current into $r_e || (R_E)$. Output side: Emitter connected to R_E (load resistor), and emitter is the output. Dependent current source (or voltage source from T-model) within the transistor. Collector is AC ground.

Derivations (using T-model for simplicity, assuming r_o is infinite and no R_C):

1. **Voltage Gain (A_v):**
    - The input voltage v_in appears across r_pi (or betar_e) and R_E.
    - Using the T-model, the voltage v_in across base-emitter path. The voltage at the emitter is essentially v_in minus the v_be drop (which is small-signal v_be).
    - v_out=i_eR_E.
    - The current through the emitter resistance is i_e=fracv_inr_e+(R_B||R_S)/beta where R_S is source resistance. For simplicity and general formula:
    - Av=vinvout=RE+reRE
    - If R_S (source resistance) is significant, it appears in series with r_pi at the input.
    - More accurately, considering source resistance R_S:
      Av=RE||ro+re+(RS||RB)/βRE||ro
      If r_o is included: v_out is across R_E||r_o. The voltage division occurs between (R_S||R_B)/beta+r_e and R_E||r_o. For the simplest case, assuming r_o=infty and no R_S in series with the base,
      Av≈re+RERE
      Since r_e is usually small compared to R_E, A_v is close to 1.
2. **Input Resistance (R_in):**
    - Looking into the base, we see r_pi in series with the impedance "reflected" from the emitter. Any resistance in the emitter appears multiplied by (beta+1) (or beta for approximation) at the base.
    - Rin=RB||[β(re+RE)]
    - (More accurately, for r_o and source impedance R_S not shorted, the formula becomes more complex, but this is the common approximation.)
    - Rin=RB||[rπ+(β+1)RE]
    - Where R_B is the Thevenin equivalent resistance of the base biasing network.
3. **Output Resistance (R_out):**
    - Looking back into the emitter, with v_in set to zero. Any source resistance R_S and bias resistor R_B at the input appear divided by beta (or beta+1) when looking into the emitter.
    - Rout=RE||[re+(RB||RS)/β]
    - Where R_S is the source resistance. If R_S=0 (ideal voltage source), then R_out=R_E||[r_e+R_B/beta].
    - Often, R_B/beta is small, so R_outapproxR_E||r_e.

Numerical Example for CC Amplifier: Consider a CC amplifier with R_E=2.2textkOmega, R_B=50textkOmega (bias resistors parallel). Transistor parameters: g_m=40textmS, r_pi=2.5textkOmega, r_e=25textOmega, beta=100. Assume r_o=infty.

1. **Voltage Gain (A_v):**
   A_v=fracR_Er_e+R_E=frac2.2textkOmega25textOmega+2.2textkOmega=frac220025+2200=frac22002225approx0.988

2. **Input Resistance (R_in):** R_in=R_B∣∣[r_pi+(beta+1)R_E]
   R_in=50textkOmega∣∣[2.5textkOmega+(100+1)2.2textkOmega]
   R_in=50textkOmega∣∣[2.5textkOmega+101times2.2textkOmega]
   R_in=50textkOmega∣∣[2.5textkOmega+222.2textkOmega]
   R_in=50textkOmega∣∣224.7textkOmega
   R_in=frac50times224.750+224.7textkOmega=frac11235274.7textkOmegaapprox40.9textkOmega
3. **Output Resistance (R_out):** Assume R_S=0 for simplicity (ideal voltage source input). R_out=R_E∣∣[r_e+R_B/beta]
   R_out=2.2textkOmega∣∣[25textOmega+50textkOmega/100]
   R_out=2.2textkOmega∣∣[25textOmega+500textOmega]
   R_out=2.2textkOmega∣∣525textOmega=2200textOmega∣∣525textOmega
   R_out=frac2200times5252200+525textOmega=frac11550002725textOmegaapprox423.8textOmega

---

3.4.4 Common Drain (CD) FET Amplifier (Source Follower)

Configuration Characteristics:

- **Input:** Applied to the gate.
- **Output:** Taken from the source.
- **Drain:** AC grounded (connected directly to VDD, which is AC ground).
- **Non-Inverting:** Output voltage is in phase with the input voltage.
- **Voltage Gain close to unity (but less than 1):** Provides current gain and impedance transformation.
- **Very High Input Resistance:** Due to the isolated gate.
- **Low Output Resistance:** Useful for driving low impedance loads.

AC Equivalent Circuit (using FET small-signal model): Input side: v_in connected to gate, R_G to gate. Gate is open circuit for current. Output side: Source connected to R_S (load resistor), and source is the output. Dependent current source (from drain to source) is within the transistor. Drain is AC ground.

Derivations (using FET small-signal model, assuming infinite r_o):

1. **Voltage Gain (A_v):**
   - The voltage at the source (v_out) is developed across R_S.
   - The dependent current source g_mv_gs flows through R_S.
   - v_gs=v_in−v_out.
   - v_out=g_mv_gsR_S=g_m(v_in−v_out)R_S
   - v_out=g_mv_inR_S−g_mv_outR_S
   - v_out(1+g_mR_S)=g_mv_inR_S
   - Av=vinvout=1+gmRSgmRS
   - If r_o is considered, R_S is in parallel with r_o when viewed from the output.
   - Av=1+gm(RS∣∣ro)gm(RS∣∣ro)
     Since g_mR_S is typically large, A_v is close to 1.
2. **Input Resistance (R_in):**

    - Looking into the gate, the resistance is the gate bias resistor(s).
    - Rin=RG
    - Where R_G is the bias resistor (or parallel combination of bias resistors).
3. **Output Resistance (R_out):**
    - Looking back into the source, with v_in set to zero (v_gs is not necessarily zero here, as v_out is connected to R_S).
    - To find R_out, apply a test voltage v_x at the output and find current i_x.
    - When v_in=0, v_gs=−v_x.
    - The current into the source is from R_S and the dependent current source.
    - The resistance seen looking into the source terminal of the FET is 1/g_m.
    - Rout=RS||(1/gm)
    - If r_o is considered, it appears in parallel as well.
    - Rout=RS||(1/gm)||ro
      Since 1/g_m is usually small, this configuration provides a very low output resistance.

Numerical Example for CD Amplifier: Consider a CD amplifier with R_S=10textkOmega, R_G=1textMOmega. Transistor parameters: g_m=4textmS, r_o=25textkOmega.

1. **Voltage Gain (A_v):** A_v=fracg_m(R_S||r_o)1+g_m(R_S||r_o) R_S||r_o=10textkOmega||25textkOmega=frac10times2510+25textkOmega=frac25035textkOmegaapprox7.14textkOmega g_m(R_S||r_o)=4textmStimes7.14textkOmega=4times10−3times7.14times103=28.56 A_v=frac28.561+28.56=frac28.5629.56approx0.966
2. **Input Resistance (R_in):** R_in=R_G=1textMOmega
3. **Output Resistance (R_out):** R_out=R_S||(1/g_m)||r_o 1/g_m=1/(4textmS)=1/(4times10−3)textOmega=250textOmega R_out=10textkOmega||250textOmega||25textkOmega First, 10textkOmega||25textkOmega=7.14textkOmega. Then, R_out=7.14textkOmega||250textOmega=7140textOmega||250textOmega R_out=frac7140times2507140+250textOmega=frac17850007390textOmegaapprox241.5textOmega This is very close to 1/g_m, indicating the dominant factor for output resistance is the transistor's inherent dynamic resistance.

3.5 Design Procedures for Specific Amplifier Specifications: Meeting Gain, Input/Output Impedance Requirements

Introduction: Designing an amplifier involves selecting appropriate transistors and component values (resistors, capacitors) to meet desired performance specifications. Small-signal analysis is indispensable in this process. The design typically starts with DC biasing to establish the Q-point, as this determines the small-signal parameters (g_m,r_pi,r_e,r_o). Then, AC analysis is used to tailor the gain and impedance characteristics.

General Design Flow:

1. **Understand Specifications:** Clearly define the required voltage gain (A_v), input resistance (R_in), and output resistance (R_out). Also consider power supply voltage, quiescent current, power dissipation, and frequency response (though we are focusing on low-frequency here).
2. **Choose Transistor Type:** Select a BJT or FET based on the application. FETs are preferred for very high input impedance, while BJTs offer higher transconductance for a given current, often leading to higher gain.
3. **Determine DC Biasing (Q-Point):**
    - **Goal:** Set the DC collector/drain current (I_C or I_D) and collector-emitter/drain-source voltage (V_CE or V_DS) to ensure the transistor is in the active/saturation region and to establish the desired small-signal parameters.
    - **Method:** Use biasing techniques (voltage divider bias, emitter feedback bias, self-bias, etc.). Often, I_C or I_D is a primary design choice as it directly impacts g_m and r_pi/r_e.
    - **Formulas:** Use DC analysis equations for the chosen bias circuit to determine resistor values (R_1,R_2,R_C,R_E for BJT; R_G,R_D,R_S for FET).
4. **Calculate Small-Signal Parameters:** Based on the chosen Q-point (I_C or I_D) and transistor parameters (beta,V_A for BJT; k′,W/L,V_th,lambda for FET), calculate g_m,r_pi,r_e,r_o.
5. **Choose Amplifier Configuration:** Select the appropriate amplifier configuration (CE, CS, CC, CD) based on the gain and impedance requirements.
    - **High Gain, Moderate R_in, Moderate R_out:** CE or CS.
    - **Unity Gain, High R_in, Low R_out (Buffer):** CC or CD.
6. **Determine AC Component Values (Resistors):**
    - **Voltage Gain:** Use the gain formulas derived in Section 3.4. For CE/CS, adjust R_C or R_D to achieve the desired gain.
        - For A_vapprox−g_mR_C (CE), if A_v is desired, then R_Capprox∣A_v∣/g_m.
        - For A_vapprox−g_mR_D (CS), if A_v is desired, then R_Dapprox∣A_v∣/g_m.
    - **Input Resistance:** For CE/CC, adjust base biasing resistors (R_1,R_2) to achieve R_in. For CS/CD, R_G directly impacts R_in.
        - For CE: R_in=R_B∣∣r_pi. If a minimum R_in is needed, R_B must be large enough. If a specific R_in is needed, you might need to adjust R_B such that R_inapproxr_pi if r_pi is dominant, or R_inapproxR_B if R_B is dominant.
        - For CS/CD: R_in=R_G. Simply choose R_G to meet the requirement.
        - For CC: R_in=R_B∣∣[r_pi+(beta+1)R_E]. This shows how R_E (and thereby I_E) and R_B affect the input impedance.
    - **Output Resistance:** For CE/CS, R_out=R_C∣∣r_o or R_D∣∣r_o. Adjust R_C or R_D to meet R_out requirements. For CC/CD, R_out=R_E∣∣[r_e+(R_B∣∣R_S)/beta] or R_S∣∣(1/g_m)∣∣r_o. This might involve choosing R_E or R_S accordingly, or understanding the inherent low output impedance of these followers.
7. **Select Coupling and Bypass Capacitors:**
    - **Purpose:** To block DC voltages while allowing AC signals to pass.

- **Rule of Thumb for Low-Frequency Cutoff:** The impedance of these capacitors should be much smaller than the resistance they are in series with at the lowest frequency of interest (f_L).
- For coupling capacitors (input C_C1, output C_C2), their reactance 1/(2pifC) should be much less than the input/output resistances they couple to.
- For bypass capacitors (C_E for CE, C_S for CS), their reactance 1/(2pifC) should be much less than the resistance they are bypassing (e.g., R_E||r_e for CE).
- Typically, choose capacitor values such that their reactance at f_L is about one-tenth of the associated resistance. This ensures they act as shorts at relevant signal frequencies.

Iterative Design: Design is often an iterative process. Initial choices might not meet all specifications simultaneously. For example, selecting I_C for a desired g_m might affect r_pi, which then impacts R_in. Adjustments to component values or even the amplifier configuration might be necessary. Simulation tools are invaluable at this stage.

Example Design Scenario (CE Amplifier): Specifications: A_vapprox−100, R_inge10textkOmega, V_CC=12textV. Use a BJT with beta=100, V_A=75textV. Assume V_T=25textmV.

1. **Choose I_C for g_m:** If A_v=−g_mR_Capprox−100, and let's initially target R_C=2.2textkOmega (a common value). Then g_mapprox100/2.2textkOmegaapprox45.45textmS. I_C=g_mV_T=45.45textmStimes25textmVapprox1.136textmA. Let's target I_C=1.2textmA. For I_C=1.2textmA: g_m=1.2textmA/25textmV=48textmS. r_pi=beta/g_m=100/48textmSapprox2.08textkOmega. r_o=V_A/I_C=75textV/1.2textmA=62.5textkOmega.
2. **DC Biasing (Voltage Divider Bias):** Assume V_CEapproxV_CC/2=6textV for maximum output swing. V_C=V_CC−I_CR_C. If we set R_C=2.2textkOmega: V_C=12textV−(1.2textmAtimes2.2textkOmega)=12textV−2.64textV=9.36textV. This is a bit high. Let's choose R_C to set V_Capprox8textV to leave some headroom. R_C=(V_CC−V_C)/I_C=(12textV−8textV)/1.2textmA=4textV/1.2textmAapprox3.33textkOmega. Use R_C=3.3textkOmega. Now calculate A_v with this R_C: A_v=−g_m(R_C||r_o)=−48textmS(3.3textkOmega||62.5textkOmega). 3.3||62.5=frac3.3times62.53.3+62.5approx3.13textkOmega. A_v=−48textmStimes3.13textkOmegaapprox−150. This gain is too high. *Adjustment:* We need to reduce the gain to -100. We can do this by either reducing R_C or by adding an unbypassed emitter resistor (R_E1). Let's try adjusting R_C first. Target |A_v|=100. So 100=g_m(R_C||r_o). 100=48textmS(R_C||62.5textkOmega). (R_C||62.5textkOmega)=100/48textmS=2.08textkOmega. fracR_Ctimes62.5R_C+62.5=2.08textkOmegaimplies62.5R_C=2.08R_C+2.08times62.5 60.42R_C=130impliesR_Capprox2.15textkOmega. Use R_C=2.2textkOmega. With R_C=2.2textkOmega, then V_C=12textV−(1.2textmAtimes2.2textkOmega)=9.36textV. This is acceptable. For biasing, assume V_E=1textV (to give good stability). R_E=V_E/I_EapproxV_E/I_C=1textV/1.2textmAapprox833textOmega. Use

R_E=820textOmega. V_B=V_E+V_BE=1textV+0.7textV=1.7textV. For voltage divider, V_B=V_CCfracR_2R_1+R_2. Set current through voltage divider to be 10timesI_B=10times(I_C/beta)=10times(1.2textmA/100)=0.12textmA. So, R_1+R_2=V_CC/0.12textmA=12textV/0.12textmA=100textkOmega. R_2=fracV_BV_CC(R_1+R_2)=frac1.7textV12textV(100textkOmega)approx14.17textkOmega. Use R_2=15textkOmega.
R_1=100textkOmega−R_2=100textkOmega−15textkOmega=85textkOmega. Use R_1=82textkOmega. Verify
R_B=R_1||R_2=82textkOmega||15textkOmegaapprox12.6textkOmega.

3. **Input Resistance check:**
R_in=R_B||r_pi=12.6textkOmega||2.08textkOmega=frac12.6times2.0812.6+2.08textkOmega=frac26.214.68textkOmegaapprox1.78textkOmega. This R_in of 1.78textkOmega is **less than** the specified 10textkOmega. This is a common issue with CE amplifiers.
Adjustment for R_in: To increase R_in, we need to either increase R_B (difficult with stability concerns and power supply voltage) or increase r_pi. Increasing r_pi means decreasing g_m, which means decreasing I_C. But decreasing I_C will also decrease gain, which we've just tried to set. The most common solution to increase R_in for a CE amplifier while maintaining gain (or controlling it) is to **add an unbypassed emitter resistor** (R_E1). Let R_E=R_E1+R_E2 (where R_E2 is bypassed). The new gain formula becomes A_v=−fracg_m(R_C||r_o)1+g_mR_E1. The new input resistance becomes R_in=R_B||[r_pi+(beta+1)R_E1].
Let's re-design with R_E1. To get R_inge10textkOmega: If we aim for R_inapprox10textkOmega, and R_B (max 100textkOmega) is limited, then we need r_pi+(beta+1)R_E1 to be significant. Let's keep I_C=1.2textmA for g_m=48textmS and r_pi=2.08textkOmega. We need r_pi+(beta+1)R_E1approx10textkOmega (if R_B is very large). 2.08textkOmega+(101)R_E1approx10textkOmega.
101R_E1approx7.92textkOmegaimpliesR_E1approx78.4textOmega. Let's use R_E1=75textOmega. Now, the voltage gain:
A_v=−frac48textmS(2.2textkOmega||62.5textkOmega)1+48textmStimes75textOmega=−frac48textmStimes2.15textkOmega1+3.6=−frac103.24.6approx−22.4. This gain is now too low! This highlights the trade-off: increasing R_in with R_E1 significantly reduces voltage gain.
Alternative approach for high gain and high R_in: If high R_in is critical, a CS amplifier might be a better choice, or a CE amplifier with a preceding CC buffer. If we must use a single CE stage, the only way to get high gain AND high R_in (without R_E1) is to use a very high beta transistor, or a much lower I_C (which makes g_m lower, reducing gain). Let's assume the user means "meet the best possible gain given the high R_in constraint for a simple CE amplifier."
Let's target R_inapprox10textkOmega. If R_in=R_B||r_pi, and we need R_inapprox10textkOmega, then r_pi must be ge10textkOmega.
r_pi=beta/g_m=betaV_T/I_Cge10textkOmega.
I_ClebetaV_T/10textkOmega=100times25textmV/10textkOmega=2.5textV/10textkOmega=0.25textmA. If we choose I_C=0.25textmA:
g_m=0.25textmA/25textmV=10textmS. r_pi=10textkOmega.
r_o=75textV/0.25textmA=300textkOmega.
Now, calculate R_C for A_v=−100:
100=g_m(R_C||r_o)=10textmS(R_C||300textkOmega).

(R_C||300textkOmega)=100/10textmS=10textkOmega. fracR_Ctimes300R_C+300=10implies300R_C=10R_C+3000implies290R_C=3000impliesR_Capprox10.34textkOmega. Use R_C=10textkOmega.
Final parameters with new I_C and R_C: I_C=0.25textmA, R_C=10textkOmega. A_v=−10textmS(10textkOmega||300textkOmega)=−10textmStimesfrac10times30010+300textkOmega=−10textmStimes9.68textkOmegaapprox−96.8. (Close enough to -100) R_in: Need to choose R_B=R_1||R_2 large enough so that R_inapproxr_pi=10textkOmega. If R_B=100textkOmega, R_in=100textkOmega||10textkOmega=9.09textkOmega. This meets the ge10textkOmega if we allow R_in to be slightly less than r_pi. To truly make R_inge10textkOmega, R_B must be very large (e.g., 1textMOmega), which might be challenging for DC stability. For instance, if R_B=1textMOmega, then R_in=1textMOmega||10textkOmegaapprox9.9textkOmega. This is very close to 10textkOmega.
This example shows the compromises and iterative nature of design.

3.6 Low-Frequency Analysis of Multistage Amplifiers: Cascading Amplifier Stages, Overall Gain Calculation

Introduction: To achieve higher overall gain, specific input/output impedance characteristics, or to combine different amplifier functions, multiple amplifier stages are often cascaded (connected in series). The low-frequency analysis of such a system involves understanding how the gain, input resistance, and output resistance of individual stages interact when connected.

Cascading Amplifier Stages: When amplifiers are cascaded, the output of one stage becomes the input of the next stage. This connection typically uses coupling capacitors to block DC biasing from one stage affecting the next, ensuring independent DC operating points.

Overall Voltage Gain Calculation: The overall voltage gain (A_v_total) of a cascaded amplifier is the product of the individual voltage gains of each stage, considering any loading effects.

Av_total=Av1×Av2×⋯×Avn

Where A_vi is the voltage gain of the i-th stage. **Important Consideration: Loading Effects.** When one stage drives another, the input resistance of the succeeding stage acts as a load on the preceding stage. This "loading" effect reduces the effective gain of the preceding stage.

The gain of a stage (A_vi) is not just the open-circuit gain, but the gain **with its specific load**. If a stage i has an open-circuit voltage gain A_vo(i) and an output resistance R_out(i), and it drives a stage i+1 with an input resistance R_in(i+1), then the actual voltage gain of stage i becomes:

Av(i)=Avo(i)×Rout(i)+Rin(i+1)Rin(i+1)

This formula represents a voltage divider formed by the output resistance of stage i and the input resistance of stage i+1.

Overall Input Resistance: The overall input resistance of the cascaded amplifier is simply the input resistance of the first stage.

Rin_total=Rin1

Overall Output Resistance: The overall output resistance of the cascaded amplifier is the output resistance of the final stage.

Rout_total=RoutN

Where N is the number of stages.

Design Strategy for Multistage Amplifiers:

1. **Stage-by-Stage Design:** Design each individual stage to meet its specific requirements (e.g., first stage for high R_in, middle stages for high gain, final stage for low R_out).
2. **Account for Loading:** When calculating the gain of each stage, explicitly include the input resistance of the next stage as its load.
3. **Overall Gain Budget:** Distribute the required overall gain among the stages. For example, if A_v_total=1000 and you have two stages, you might aim for A_v1=30 and A_v2=33.3.
4. **Impedance Matching:** Often, the first stage is designed for high input impedance to avoid loading the signal source, and the last stage is designed for low output impedance to efficiently drive a load. Intermediate stages might prioritize voltage gain.

Numerical Example for Multistage Amplifier: Consider a two-stage amplifier: **Stage 1: CE Amplifier**

- Open-circuit voltage gain A_vo1=−200
- Output resistance R_out1=5textkOmega
- Input resistance R_in1=10textkOmega

Stage 2: CC Amplifier (Emitter Follower)

- Open-circuit voltage gain A_vo2=0.98 (this is already close to the loaded gain for CC)
- Output resistance R_out2=50textOmega
- Input resistance R_in2=50textkOmega

Let the signal source have R_S=1textkOmega. Let the final load be R_L=1textkOmega.

1. **Input Resistance of the overall amplifier:** R_in_total=R_in1=10textkOmega
2. **Output Resistance of the overall amplifier:** R_out_total=R_out2=50textOmega
3. **Voltage Gain of Stage 1 (considering load from Stage 2):** The load for Stage 1 is R_in2=50textkOmega.

A_v1=A_vo1timesfracR_in2R_out1+R_in2=−200timesfrac50textkOmega5textkOmega+50textkOmega A_v1=−200timesfrac5055=−200times0.909approx−181.8

4. **Voltage Gain of Stage 2 (considering final load R_L):** The load for Stage 2 is R_L=1textkOmega. A_v2 for a CC amplifier is already typically calculated with its load in mind. The formula A_v=fracR_Er_e+R_E from earlier implicitly includes the load R_E. If R_L is the final external load on the emitter, then R_E in that formula is effectively replaced by R_E∣∣R_L. For simplicity, let's assume A_v2 given (0.98) is the gain when driving R_L=1textkOmega. If not, we'd need to re-evaluate it with R_L.
5. **Overall Voltage Gain (A_v_total):** A_v_total=A_v1timesA_v2=−181.8times0.98approx−178.16